

ABSTRACT

Chip area corresponding to unnecessary I/O cell sites is recovered and made usable for additional core cells and power connections by grouping I/O cells into I/O kernels of contiguous I/O cells having power connections independent of other I/O kernels and depopulating I/O cell sites in accordance with areas corresponding to I/O kernels. Since I/O kernels have dedicated power connections, no power busses are present in the depopulated I/O cell sites which can then be freely use for additional core cells, power connections or the like. This technique also allows selection of a chip of minimum required area to be determined prior to design of chip layout.